

Current-Transformer Phase-Shift Compensation and Calibration

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ABSTRACT

This application report demonstrates a digital technique to compensate and calibrate the phase shift of a current (or voltage) transformer used in electric power or energy measurement. Traditional analog compensation is replaced by a digital finite impulse response (FIR) filter. A technique emulating a non-unity power factor (non-UPF) load makes the calibration fully automatic. The calibration time is greatly reduced and it is more accurate and consistent. Use of emulation removes the bulky expensive non-UPF load. The 16-bit RISC MSP430 mixed-signal processor from Texas Instruments is an effective means of handling the otherwise demanding computational requirements.

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1 Introduction

Current transformers (CTs) are commonly used in electricity meters for current measurement, and to provide isolation when direct coupling is not possible. However, all CTs include an inherent phase shift that changes the power factor of its output. Inductive and capacitive loads cause the measured ac power error to increase significantly and unacceptably as the mains power factor decreases.

An analog RC filter is the traditional way to overcome the phase shift problem; however, RC filters are not very satisfactory because of their cost, stability issues, and the need for time consuming manual calibration. These drawbacks are overcome with digital compensation and automated calibration.

This application report consists of two parts: compensation and calibration. The section on compensation describes the design of a single zero-finite impulse response (zero-FIR) filter. This filter provides a group delay to compensate for the CT's phase shift. Unfortunately, it also alters the dc gain, and this needs to be corrected.

The section on calibration shows how to calculate the FIR parameters for various delays, then deals with emulating a non-UPF load, determining the non-UPF error, and locating the actual FIR parameters used.

2 Digital Phase Shift Compensation

2.1 Problem Description

Because of inductive and capacitive loading, ac mains voltage and current are sometimes out of phase, so when a CT is used, the measured current has a phase lead (or lag) over the original current.

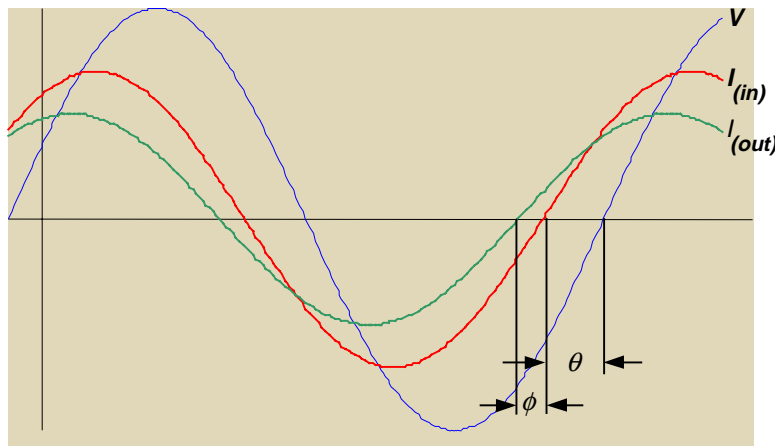


Figure 1. CT Phase Response

In Figure 1, the input mains current, $I_{(in)}$, leads the voltage, V , by θ and the output current, $I_{(out)}$ further leads $I_{(in)}$ by ϕ . The actual power is

$$P = V_O I_O \cos \theta \quad (1)$$

where V_O is the maximum ac input voltage, I_O is the maximum ac input current, and $\cos \theta$ is the power factor. The measured power is

$$P' = K_{(V)} V'_O K_{(I)} I'_O \cos(\theta + \phi) \quad (2)$$

where $K_{(V)}$ is the scale-down factor for voltage ($V_O = K_{(V)} V'_O$), $K_{(I)}$ is the scale-down factor for current ($I_O = K_{(I)} I'_O$), and $\cos(\theta + \phi)$ is the measured power factor. Thus, the measured error is

$$E_{(m)} = 1 - \frac{P'}{P} = 1 - \frac{\cos(\theta + \phi)}{\cos \theta} \quad (3)$$

The error is a nonlinear function of the power factor. For a UPF load, ϕ is usually small and the error can be ignored; however, as the power factor decreases, the error becomes significant. For example, with a power factor of 0.5 and a phase shift of 1° , the error is an unacceptable 3%.

2.2 FIR Filter

To overcome the problem of phase shift across the CT, the output current could be delayed by the same amount as the inherent phase shift so that both the actual and measured power factors were equal. However, this delay would probably not be a multiple of the sampling time, so the problem could not be solved simply by adding one or more sample delays.

A simple way to provide fractional delay is to use a single zero-FIR filter:

$$y[n] = x[n] + \beta x[n-1] \quad (4)$$

Here x is input current, y is delayed output current, n is sampling sequence, and β is delay gain.

The frequency response can be derived in z-transform space from which the filter's group delay, D , is the derivative of the angular response:

$$D = \frac{\beta(\beta + \cos \omega)}{1 + \beta^2 + 2\beta \cos \omega} \quad (5)$$

where ω is the angular frequency after sampling, equal to $2\pi \times (\text{mains frequency})/(\text{sampling frequency})$

Solving equation (5) for β gives:

$$\beta = -\frac{(1-2D)\cos \omega \pm \sqrt{(1-2D)^2 \cos^2 \omega + 4D(1-D)}}{2(1-D)} \quad (6)$$

The phase shift is actually the group delay of the angular plane. They are related by

$$D = \phi/\omega \quad (7)$$

where the phase shift, ϕ , is measured in radians. To compensate for the non-unity gain of the filter, the output is multiplied by the inverse of the filter gain, which is:

$$A^{-1} = [(\cos \omega + \beta)^2 + \sin^2 \omega]^{-1/2} \quad (8)$$

For example, for an e-meter design with a sampling frequency of 995.025 Hz, an input mains frequency of 50 Hz, and a CT phase shift of 1° , $\beta = 0.0611975$, and $A^{-1} = 0.944873$.

3 CT Calibration

Linear calibration should be done first because it affects the CT calibration. On the other hand, CT phase shift has almost no impact on linear calibration.

The actual CT calibration starts by internally delaying the mains input current to emulate a non-UPF load. This is the main technique used in the whole calibration process. A small CT phase shift creates a relatively big error in this case. Errors for a range of CT delays and parameters for the corresponding compensation FIR are pre-calculated and put into tables. The error produced with the emulated non-UPF load is measured using a reference meter. The correct FIR coefficients can then be identified by a table lookup.

3.1 Non-UPF Load Emulation

Because the CT phase shift is usually small, equation (3) shows that the error is very small under UPF load. Therefore, a large capacitor or inductor would be required in order to obtain the large errors needed for an accurate calibration.

The use of internal delay to emulate this non-UPF load not only removes the necessity for these expensive and bulky loads, but it also makes the calibration process automatic by requiring only a single UPF load.

The delaying of current (or voltage) input is equivalent to changing the power factor so that a non-UPF load can be emulated. There is no strict requirement on the value of the emulated non-UPF load—it needs only to be big enough for accurate calibration (but not so large as to give a very small power factor). For ease of implementation, the delay can be chosen as a multiple of the sampling time. The phase delay, ξ , is:

$$\xi = \frac{f_{(m)}}{f_{(s)}} \times N \quad (9)$$

where $f_{(m)}$ and $f_{(s)}$ are the mains and sampling frequencies, respectively, and N is the number of delayed samples.

The factor $\cos \xi$ is the emulated power factor. As an example, consider a mains frequency of 50 Hz, sampled at 995.025Hz. A three-sample delay gives a phase delay of 54.27°, perfectly adequate for calibration.

3.2 Calculation of Error

There are a number of ways to get a reference input from an external reference meter. The method used here is simple: the reference meter produces LED pulses with a frequency proportional to the measured energy. For example, a rate of 1600 pulses/hr for each kilowatt-hour means that 1600 pulses will be produced in one hour with a one-kilowatt load. A simple optical sensor can be used to couple the LED pulses to the meter under calibration. This method provides a very simple interface and requires only one input line. It is assumed that the meter under calibration produces LED pulses in the same manner as the reference meter.

The error caused by the CT phase shift is obtained by normalizing the difference in times needed for the same number of pulses to be emitted by the reference input and the meter internal generated. This is the pulse-time error, $E_{(P)}$, not the error in energy or power defined by equation (3):

$$E_{(P)} = (t'_{(int)} - t_{(ref)}) / t_{(ref)} \quad (10)$$

where $t'_{(int)}$ is the modified internal pulse time ($= t_{(int)} / \cos \xi$), $t_{(int)}$ is the measured internal pulse time, and $t_{(ref)}$ is the reference pulse time. Note that because the external reference does not experience the internal emulated delay, it is necessary to convert the internal time back to UPF conditions by dividing by the emulated power factor.

3.3 Setting Up the FIR Parameters Table

FIR parameters for a given phase shift can be calculated using equations (6) to (8). The calculations are best done in a spreadsheet, thereby determining an entire pre-calculated table. The tolerance of the CT phase shift must be known to determine the maximum and minimum phase shift. The phase shift step is chosen so that the error due to inexact compensation remains acceptable. For example, if the step size is 0.1° and the minimum power factor is $\cos(60^\circ) = 0.5$, the maximum error is $1 - [\cos(60^\circ + 0.1^\circ) / \cos(60^\circ)] = 0.3\%$.

Using the second definition of the phase time error in equation (10) gives:

$$E_{(P)} = \frac{\cos \xi}{\cos(\xi - \phi)} - 1 \quad (11)$$

To minimize the program code size and the search time, an implicit table for $E_{(P)}$ can be used. The errors, $E_{(max)}$ and $E_{(min)}$, corresponding to the maximum and minimum phase shift are calculated first. Then the phase-shift step-size is translated into the error step-size:

$$E_{(step)} = \frac{E_{(max)} - E_{(min)}}{\text{Total number of steps}}$$

For each value of $E_{(P)}$, the actual phase shift is calculated from equation (10), and the result is used in equations (6) to (8) to give the final FIR parameters. Because $E_{(P)}$ can be easily calculated from $E_{(min)}$ and $E_{(step)}$, it does not need to be stored—only $E_{(max)}$, $E_{(min)}$ and $E_{(step)}$ are retained.

3.4 CT With Large Phase Shift

In some cases, there are CTs with relatively large inherent phase shifts. For example, high mains frequencies or low sampling frequencies increase the phase shift of even a CT with an inherently small phase shift. This is in conformity with equation (7).

CTs with a large phase shift can still be compensated and calibrated provided they exhibit a mean phase shift with an acceptable range of deviation. This kind of CT can be compensated first with an FIR designed for a mean phase shift η under UPF calibration. If η is more than the phase delay of a single sample, then a combination of multiple and fractional sample delays can be used, the fractional delays being derived from an FIR. In that case:

$$\eta = N_{(d)}\psi + \zeta \quad (12)$$

where ψ is the phase delay of a single sample ($= [\text{mains frequency}] / [\text{sampling frequency}]$) and $N_{(d)}$ is the number of delayed samples with $\zeta < \psi$. The CT phase shift is then:

$$\phi' = \phi - \eta \quad (13)$$

where ϕ is the original CT phase shift. Because ϕ' is very small, it can be ignored in the UPF calibration.

After the UPF calibration, calibration continues with the emulated non-UPF load. However, now the equivalent phase shift, ϕ' , is compensated instead of the original CT phase shift, ϕ . The equivalent emulated phase delay, ξ' , for ϕ' is:

$$\xi' = \xi - \eta \quad (14)$$

where ξ is the actual emulated phase delay added and η is the mean CT phase shift. The same technique as before can now be used to calibrate ϕ' .

3.5 Variation of Mains Frequency

It is important that the actual mains frequency match the frequency of calibration. Any deviation causes a calibration error on the CT phase shift. However, once calibration is completed, the FIR compensation maintains its accuracy even under different mains frequencies.

4 Summary

In general, digital techniques have an advantage over analog in terms of accuracy and consistency; however, this often comes at a higher cost. The method outlined in this application report uses digital techniques for compensating and calibrating a CT and yet is simple enough to be implemented in a low cost microcontroller. The solution has been successfully implemented in a Texas Instruments MSP430 microcontroller and has passed a national approval for class-1 electricity meters.

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